

FIG. 1

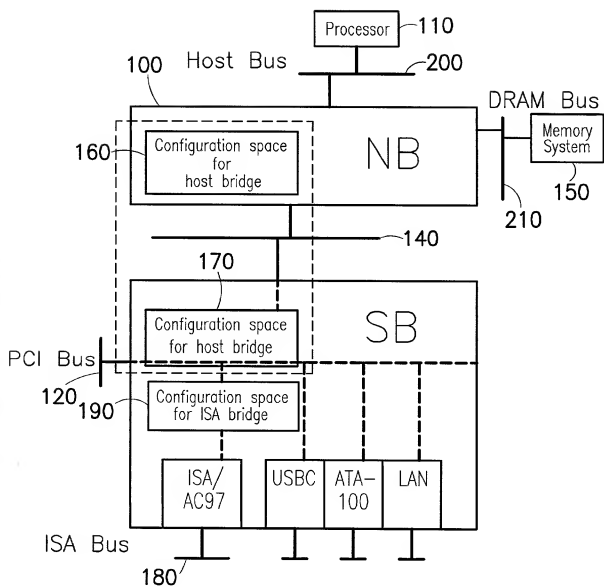


FIG. 2

FIG. 3 is a block diagram of a system architecture showing a Host Bus (200) connected to a Processor (110) and a Memory System (150). The Host Bus (200) is connected to a North Bridge (NB) (100) and a South Bridge (SB) (130). The North Bridge (NB) (100) contains a selection logic (260) and a multiplexer (220, 230). The South Bridge (SB) (130) contains a selection logic (240, 250) and a Configuration space for ISA bridge (120). The North Bridge (NB) (100) is connected to the South Bridge (SB) (130) via a bus (140). The North Bridge (NB) (100) is also connected to the Host Bus (200) via a bus (210).

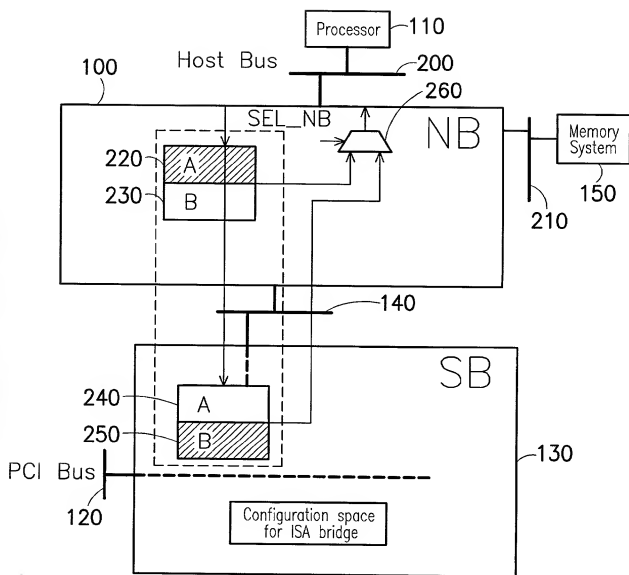


FIG. 3